

## Description

# METHODS FOR MANUFACTURING A FINFET USING A CONVENTIONAL WAFER AND APPARATUS MANUFACTURED THEREFROM

### BACKGROUND OF INVENTION

- [0001] The present invention relates generally to the field of semiconductor manufacturing. More particularly, the present invention relates to fin field effect transistors and a method for manufacturing the same.
- [0002] The need to remain cost and performance competitive in the production of semiconductor devices has driven integrated circuits to increased device density. To facilitate the increase in device density, new technologies are constantly needed to allow the feature size of these semiconductor devices to be reduced.
- [0003] The push for ever increasing device densities is particularly strong in CMOS technologies such as in the design

and fabrication of field effect transistors (FETs). FETs are the dominant components of complementary metal oxide semiconductors (CMOS). Scaling FETs to attain higher device density in CMOS results in degradation of short channel effect and/or reliability.

[0004] One type of FET that has been proposed to improve short channel effect and facilitate increased or not decrease device density is a fin Field Effect Transistor ("finFET"). In finFETs, the body of the transistor is formed from a vertical structure, generally referred to as a "fin" for its resemblance to the dorsal fin on a fish. The gate of the finFET is then formed on one or more sides of the fin. FinFETs have several advantages, including better current control without requiring increased device size. FinFETs thus facilitate scaling of CMOS dimensions while maintaining an acceptable performance.

[0005] FinFETs are generally produced using silicon-on-insulator (SOI) wafers. While the use of SOI wafers provides needed isolation for finFETs, it is not without significant drawbacks. The most compelling drawback of forming finFETs from SOI wafers is the added costs for SOI wafers compared to bulk silicon wafers. For example, SOI wafers can commonly cost two to three times the cost of bulk silicon

wafers. This increased cost of SOI wafers, while acceptable for some applications, is prohibitive in others. Additionally, the use of SOI wafers is not compatible with all fabrication processes, such as commonly used SiGe processes.

[0006] Thus, there is a need for a method of producing finFETs using the lesser expensive bulk semiconductor substrates.

#### **SUMMARY OF INVENTION**

[0007] It is an object of the present invention to provide a method of producing a fin structure for a finFET.

[0008] It is another object of the present invention to provide a method of producing a fin structure for a finFET that is cost effective.

[0009] It is yet another object of the present invention to provide a method of producing a fin structure for a finFET without the use of an SOI wafer.

[0010] It is still yet another object of the present invention to provide a method of producing a fin structure for a finFET using conventional bulk semiconductor materials.

[0011] It is a further object of the present invention to provide a method of producing a fin structure for a finFET using a Si/SiGe/Si substrate.

[0012] It is yet a further object of the present invention to provide a fin structure for a field effect transistor comprising

a silicon fin attached to a support structure, the support structure attached to a semiconductor substrate such that a void exists between the silicon fin and the semiconductor substrate.

[0013] To accomplish the foregoing objects and advantages, the present invention, in brief summary, is a method of producing a fin structure on a semiconductor substrate using an epi strained thin SiGe layer to produce a void between a silicon substrate and a silicon fin portion, and a fin structure produced thereby.

#### **BRIEF DESCRIPTION OF DRAWINGS**

[0014] Figures 1 shows a cross sectional view of an Si/SiGe/Si structure.

[0015] Figure 2 shows a perspective view of a fin portion of a silicon layer and a portion of an SiGe layer defined above a semiconductor substrate, and a support structure attached to the fin portion and the semiconductor substrate.

[0016] Figure 3 shows a perspective view of a fin portion of a silicon layer suspended above a semiconductor substrate with a void there between.

[0017] Figures 4 to 13 show cross sectional views of portions of a semiconductor structure at various stages of an embodi-

ment of a method of the present invention.

[0018] Figures 14 to 22 show cross sectional views of portions of a semiconductor structure at various stages of another embodiment of a method of the present invention.

[0019] Figures 23 to 28 and 30 show cross sectional views and Figures 29 and 31 show top views, of portions of a semiconductor structure at various stages of yet another embodiment of a method of the present invention.

#### **DETAILED DESCRIPTION**

[0020] The present invention provides a method of producing a fin structure on a semiconductor substrate using a thin SiGe layer to produce a void between a silicon substrate and a silicon fin portion. A portion of silicon layer in the shape of the desired fin structure is suspended above the semiconductor substrate by a supporting structure, while a portion of the SiGe layer is removed to form a void that either remains as a void in the completed FinFET or is filled with an insulating material.

[0021] The use of conventional wafers, such as a silicon wafer, in the method of the present invention decreases the cost of producing FinFET's over the use of an SOI substrate. The method of the present invention also allows for the production of fin widths that are smaller than what is possi-

ble using traditional photolithography. Using photolithography alone, widths of fin structures are limited by the resolution of the photolithography, typically 30 nanometers (nm). However, the method of the present invention allows for fin widths at least as narrow as about 10 nm, without the use of the more expensive SOI techniques.

[0022] Referring to the drawings and, in particular Figure 1, a conventional semiconductor substrate generally represented by reference numeral 102, such as a conventional silicon wafer, is provided. On the semiconductor substrate 102 is a thin silicon germanium (SiGe) layer 104. The SiGe layer 104 may be an epitaxial grown layer. The SiGe layer 104 is a single crystal layer, which is strained to provide a matching lattice constant to the semiconductor substrate 102. On the SiGe layer 104, opposite semiconductor substrate 102, is provided a silicon layer 106. The silicon layer 106 can also be a single crystal layer. These three components provide an Si/SiGe/Si structure 100, as shown in Figure 1. In another embodiment (not shown), the SiGe layer 104 is produced by germanium implantation in a conventional silicon semiconductor wafer. High temperature annealing is used to remove implantation damage and to form a layer of buried SiGe in the silicon

wafer to provide the Si/SiGe/Si structure 100 having a semiconductor substrate 102, an SiGe layer 104, and a silicon layer 106.

[0023] The layer thickness for semiconductor substrate 102 can be any thickness that is mechanically strong enough to support a chip.

[0024] The layer thickness for SiGe layer 104 can be from about 10 nm to about 30 nm. Preferably, the layer thickness for SiGe layer 104 can be from about 20 nm to about 25 nm. More preferably, the layer thickness for SiGe layer 104 can be from about 20 nm to about 25 nm.

[0025] The layer thickness for silicon layer 106 can be from about 30 nm to about 100 nm. Preferably, the layer thickness for silicon layer 106 can be from about 40 nm to about 80 nm. More preferably, the layer thickness for silicon layer 106 can be from about 50 nm to about 70 nm.

[0026] In Figure 2, fin portion 124 of silicon layer 106 has thereunder a second portion 126 of SiGe layer 104. A support structure 105 is connected to fin portion 124 and semiconductor substrate 102. Any support structure that suspends the fin portion 124 above the semiconductor substrate 102 while the second portion 126 of SiGe layer 104 is removed, is suitable. Support structure 105 can be re-

moved prior to completion of the fin structure or can be an integral part of a completed FinFET.

[0027] In Figure 3, second portion 126 of SiGe layer 104 is removed to form a first void 130 between fin portion 124 and semiconductor substrate 102. In one aspect of the present invention, a completed fin structure may retain the first void 130. In another aspect of the present invention, first void 130 may be filled with an insulating material, such as a nitride, an oxide, a low-k dielectric, or any combinations thereof.

[0028] Figures 4 to 13 show cross sectional views of portions of a semiconductor structure at various stages of an embodiment of a method of the present invention. An Si/SiGe/Si structure 100, as in Figure 1, is provided. Referring to Figure 4, silicon layer 106, opposite SiGe layer 104, has a first blocking layer 110 deposited thereon. The poly-silicon layer 112 may have a layer thickness from about 70 nm to about 120 nm. Examples of suitable materials for the poly-silicon layer 112 include, but are not limited to, poly-silicon, poly-silicon/germanium, nitride, or any combinations thereof.

[0029] When the poly-silicon layer is only a poly-silicon, the use of a second blocking layer on the poly-silicon layer 112



can protect the portions of the poly-silicon layer during subsequent etching. Poly-silicon/germanium has a different etch rate and does not require the use of an additional blocking layer on the poly-silicon layer 112.

[0030] Examples of materials that can be used in or for the first blocking layer 110 include, but are not limited to, a nitride, an oxide, oxynitride, or any combinations thereof. The layer thickness for first blocking layer 110 can be from about 5 nm to about 10 nm. Preferably, the layer thickness for first blocking layer 110 can be from about 8 nm to about 10 nm. More preferably, the layer thickness for first blocking layer 110 can be from about 9 nm to about 10 nm.

[0031] With reference to Figure 5, poly-silicon layer 112 and the first blocking layer 110 are patterned to reveal a first portion 114 of silicon layer 106 and a first portion 116 of the SiGe layer 104. This patterning also produces a sidewall 118 of the poly-silicon layer 112 and a sidewall 120 of the first blocking layer 110.

[0032] Referring to Figure 6, the sidewalls 118 and 120 of the poly-silicon layer 112 and first blocking layer 110, respectively, have deposited or formed thereon a first spacer 122. The first spacer 122 may have any suitable

material to act as a mask to cover and define thereunder a second portion 124 of the silicon layer 106 and a second portion 126 of the SiGe layer 104. The second portion 124 of the silicon layer 106 will form a part of the fin structure. An example of a material for the first blocking layer includes, but is not limited to, a nitride.

[0033] Referring to Figure 7, the first portion 114 of silicon layer 106, as in Figure 6, is removed revealing a first sidewall 128 of second portion 124 of silicon layer 106 and leaving the second portion 124 of silicon layer 106. Examples of suitable ways to remove the first portion 114 of silicon layer 106 include, but are not limited to, etching, reactive ion etch (RIE), or any combinations thereof.

[0034] The first portion 116 of SiGe layer 104, as in Figure 6, is removed revealing a first sidewall 129 of SiGe layer 104. Examples of suitable ways to remove the first portion 116 of SiGe layer 104 include, but are not limited to, etching, reactive ion etch, or any combinations thereof. Removal of the first portion 116 of SiGe layer 104 is done selective to the material of semiconductor substrate 102, such that the material of the semiconductor substrate 102 is not removed during the step of removing the first portion 116 of SiGe layer 104.

[0035] The second portion 126 of SiGe layer 104, as shown in Figure 7, is removed revealing a first void 130, as shown in Figure 8, between the semiconductor layer 102 and the second portion 124 of silicon layer 106. Examples of suitable ways to remove second portion 126 of SiGe layer 104 include, but are not limited to, wet etching, RIE, or any combinations thereof. The first void 130 has the volume under the second portion 124 of silicon layer 106. However, additional material of SiGe layer 104 may also be removed during this step. The removal is done selective to the material of semiconductor substrate 102. Some of the second portion 126 of SiGe layer 104 may have already been removed during the step of removing first portion 116 of SiGe layer 104. The remaining SiGe layer 104, silicon layer 106, first blocking layer 110, and poly-silicon layer 112 act to support second portion 124 of silicon layer 106 over first void 130.

[0036] In Figure 9, a first insulating material 134 is deposited in the first void 130, on the sidewall 128 of second portion 124 of silicon layer 106, and on the first spacer 122. Examples of suitable materials for use in or for first insulating material 134 include, but are not limited to, an oxide, a nitride, oxynitride, low-k material, or any combinations

thereof.

[0037] In Figure 10, a third blocking layer 135 is deposited on first insulating material 134 in order to block subsequent removal of first insulating material 134 during the removal of poly-silicon layer 112 and first blocking layer 110. Examples of suitable materials for use in or for third blocking layer 135 include, but are not limited to, poly-silicon, poly-silicon germanium, or any combinations thereof. The thickness of the third blocking layer 135 is preferably greater than the sum of the thicknesses of the SiGe layer 104, silicon layer 106, first blocking layer 110, and poly-silicon layer 112.

[0038] Figure 11 shows the result of chemical mechanical polishing (CMP) which stops on the top of first spacer 122. This removes first insulating material 134 that is covering the poly-silicon layer 112, and any optional second blocking layer.

[0039] Referring to Figures 11 and 12, poly-silicon layer 112, part of third blocking layer 135, and first blocking layer 110 that remain, as in Figure 11, are removed. Examples of suitable ways to remove poly-silicon layer 112 and first blocking layer 110 include RIE or any conventional dry etch methods. The portion of silicon layer 106 in Figure

11 that is not part of second portion 124 is removed, revealing a second sidewall 136 of second portion 124 of silicon layer 106, as seen in Figure 12. An example of a suitable way to remove portions of silicon layer 106 that are not part of second portion 124 includes, but is not limited to, RIE. The remaining SiGe layer 104, as in Figure 11, is removed. Preferably, this removal is done selective to the material of semiconductor layer 102. Examples of suitable ways to remove remaining SiGe layer 104 include, but are not limited to, wet etching, RIE, or any combinations thereof.

[0040] At this point or at a later time, any excess first insulating material 134 covering semiconductor substrate 102 can also be removed. Insulating material 134 will be used to support second portion 124 of silicon layer 106 and first spacer 122 upon the removal of the remaining polysilicon layer 112, remaining first blocking layer 110, remaining silicon layer 106 that is not a part of second portion 124, and remaining SiGe layer 104. Enough first insulating material 134 must remain to perform this function.

[0041] Referring to Figures 9 and 10, first insulating material 134 that is not under second portion 124 of silicon layer 106 (that part that is in the first void) is removed. Examples of

suitable ways to remove such first insulating material 134 include, but are not limited to, wet etching, dry etch, or any combinations thereof. In one aspect of the present invention, the first insulating material 134 is asymmetrical as shown in Figure 13.

[0042] When the first insulating material 134 is suitable for use as a gate insulating material, such as a gate oxide, it may be desirable to leave first insulating material 134 that is not under second portion 124 of silicon layer 106. In that situation, a second insulating material (not shown) may be deposited using a suitable technique, such as high density plasma deposition (HDP) on side wall 136 of second portion 124 of silicon layer 106 and other surfaces, such as semiconductor substrate 102 and first spacer 122, prior to etching and formation of FinFET using conventional processes.

[0043] In another embodiment of the present invention, a fin structure is produced using a method similar to that described above. Referring to Figures 1, 4 to 7 and 14 to 22, cross sectional views of semiconductor structures at various stages of a method of producing a fin structure are shown. The method involves the same steps as described in the embodiment above up to and including the removal

of first portion 116 of SiGe layer 104 as in Figure 7. Thereafter, on sidewall 118 of poly-silicon layer 112, sidewall 120 of first blocking layer 110, sidewall 128 of second portion 124 of silicon layer 106, and sidewall 129 of second portion 126 of SiGe layer 104, a second spacer 140 is formed as shown in Figure 14. The second spacer 140 can be of the same or different material as first spacer 122 of Figure 6. The second spacer 140 can be formed after the removal of all or part of the first spacer or can be formed on top of the existing first spacer. The second spacer 140 can include any suitable material for supporting second portion 124 of silicon layer 106 upon the removal of poly-silicon layer 112, first blocking layer 110, the portion of silicon layer 106 not part of second portion 124, and SiGe layer 104, as will be described in detail below. Examples of materials for use in or for second spacer 140 include, but are not limited to, a nitride, oxynitride, or any combinations thereof.

[0044] In Figure 15, first insulating material 134 is deposited on semiconductor substrate 102, second spacer 140, and poly-silicon layer 112. Third blocking layer 135 is deposited on first insulating material 134.

[0045] Figure 16 shows the result of chemical mechanical polish-

ing (CMP) of third blocking layer 135 and first insulating material 134 stopping on the top of second spacer 140.

[0046] Referring to Figures 16 and 17, any optional second blocking layer material (not shown) remaining on poly-silicon layer 112 is removed. Remaining poly-silicon layer 112, third blocking layer 135, and first blocking layer 110 are removed. This removal may be by any suitable way. Examples of ways to remove poly-silicon layer 112 and first blocking layer 110 include, but are not limited to, RIE, dry etch, or any combinations thereof. The portions of silicon layer 106 that are not part of second portion 124 are removed, revealing a second sidewall 136 of second portion 124 of silicon layer 106, as in Figure 17. This removal may be by any suitable way. Examples of ways to remove portions of silicon layer 106 that are not part of second portion 124 include, but are not limited to, RIE, dry etch, or any combinations thereof.

[0047] The first insulating material 134, as in Figure 14, is removed from first spacer 140 and from semiconductor substrate 102. The SiGe layer 104 that remains, as in Figure 16, is removed. This removal may be done by any suitable way. Preferably, this removal is done selective to the material of semiconductor layer 102. Examples of



ways to remove remaining SiGe layer 104 include, but are not limited to, wet etching, RIE, or any combinations thereof. In one aspect, this removal of the remaining SiGe layer 104 may be done by wet etching, selective to the material of semiconductor substrate 102, to remove the SiGe layer 104 including the second portion 126 of SiGe layer 104 to produce a first void 130 beneath second portion 124 of silicon layer 106 and above semiconductor substrate 102, as in Figure 17. Second spacer 140 acts as a supporting structure to suspend second portion 124 of silicon layer 106 over semiconductor substrate 102 with first void 130 there between.

[0048] The removal of the remaining SiGe layer 104 may also be done in a step-wise fashion, thereby first removing SiGe layer 104 that is not a part of second portion 126 of SiGe layer 104 first. This removal may be done by etching that part of the SiGe layer 104 selective to the material of the semiconductor layer 102 leaving second portion 126 of SiGe layer 104 in place, as in Figure 18. Next, enough heat to induce oxidation of the second portion 126 of SiGe layer 104 is applied. An example of an appropriate level of heat to induce oxidation includes, but is not limited to, about 1,000° Celsius (C) to about 1,200° C. It is believed

that the SiGe oxidation occurs at a rate that is much larger (approximately 3.5 times faster) than that of pure silicon, such that the second portion 126 of SiGe layer 104 will turn to oxide earlier than the second portion 124 of silicon layer 106 and the semiconductor substrate 102. Figure 19 shows the formation of oxidation material 150. The oxidation material 150 is then removed, as in Figure 20, to reveal first void 130. Second portion 124 of silicon layer 106 is suspended above the semiconductor substrate 102 by the support mechanism of the second spacer 140. Second spacer 140 acts as a supporting structure to suspend second portion 124 of silicon layer 106 over semiconductor substrate 102 with first void 130 therebetween.

[0049] Referring to Figure 21, in first void 130 of Figure 17 or 20, a first insulating material 152 is deposited. Examples of suitable ways for depositing first insulating material 152 include, but are not limited to, direct deposition, HDP, or any combinations thereof. Examples of materials for use in or for the first insulating material include, but are not limited to, an oxide, a nitride, low-k material, or any combinations thereof.

[0050] Referring to Figures 21 and 22, second spacer 140, as in

Figure 21, is removed. This removal of second spacer 140 may be done by any suitable way. Examples of ways to remove second spacer 140 include, but are not limited to, wet etching, dry etch, or any combinations thereof. The first insulating material 152 that is not in first void 130, as in Figure 21, is removed. This removal may be done by any suitable way. Examples of ways to remove such first insulating material 134 include, but are not limited to, RIE, dry etch, or any combinations thereof. This produces a fin structure 154, as in Figure 22, on semiconductor substrate 102. Thereafter, conventional processes for forming a FinFET can be followed.

[0051] In yet another embodiment, an Si/SiGe/Si structure 100, as in Figure 1, is provided. Referring to Figure 23, on silicon layer 106 is deposited a first blocking layer 160. Examples of materials for use in or for the first blocking layer 160 include, but are not limited to, a nitride, oxide, or any combinations thereof. The layer thickness for first blocking layer 160 is from about 5 nm to about 20 nm. Preferably, the layer thickness for first blocking layer 160 is from about 8 nm to about 15 nm. More preferably, the layer thickness for first blocking layer 160 is from about 8 nm to about 10 nm.

[0052] On first blocking layer 160, opposite silicon layer 106, is deposited a first photoresist material 162. The layer thickness for first photoresist material 162 is from about 100 nm to about 400 nm. Preferably, the layer thickness for first photoresist material 162 is from about 150 nm to about 300 nm. More preferably, the layer thickness for first photoresist material 162 can be from about 200 nm to about 250 nm.

[0053] Referring to Figure 24, the first photoresist material 162 is patterned to form the pattern of the desired fin structure with second portion 124 of silicon layer 106 and second portion 126 of SiGe layer 104 defined under the pattern.

[0054] The first blocking layer 160 not beneath the first photoresist material 162 is removed. The first blocking layer 160 may be removed by any suitable way. Examples of ways to remove first blocking layer 160 include, but are not limited to, RIE, dry etch, or any combinations thereof.

[0055] Referring to Figures 24 and 25, the silicon layer 106 not part of second portion 124 of silicon layer 106 and SiGe layer 104 not part of second portion 126 of SiGe layer 104 are removed by any suitable way to leave second portion 124 of silicon layer 106 having a first sidewall 164 and a

second sidewall 168. The second portion 124 of silicon layer 106 is the fin portion that will be suspended above semiconductor substrate 102 in the steps below. Examples of ways for removing silicon layer 106 and SiGe layer 104 include, but are not limited to, RIE, dry etch, or any combinations thereof. Preferably, the removal of silicon layer 106 is selective to the material of SiGe layer 104 and the removal of SiGe layer 104 is selective to the material of semiconductor layer 102.

[0056] Referring to Figure 26, the remaining first photoresist material 162, as in Figure 25, is removed. Examples of suitable ways to remove first photoresist material 162 include, but are not limited to, etching.

[0057] Semiconductor substrate 102 and, optionally, first blocking layer 160, have a first insulating material 170 deposited thereon. Preferably, first insulating material 170 is deposited by high density plasma (HDP) deposition. This method results in thicker oxide on the top of semiconductor substrate 102 and first blocking layer 160, but thinner oxide on first and second sidewalls of second portion 124 of silicon layer 106. Examples of materials suitable for use in or for first insulating material 170 include, but are not limited to, an oxide, a nitride, or any combi-

nations thereof. After the HDP, any first insulating material 170 on first and second sidewalls of second portion 124 of silicon layer 106 are removed to expose the sidewall for formation of gate insulating material 172.

[0058] The layer thickness for first insulating material 170 is from about 10 nm to about 50 nm. Preferably, the layer thickness for first insulating material 170 is from about 10 nm to about 30 nm. More preferably, the layer thickness for first insulating material 170 is from about 25 nm to about 30 nm.

[0059] On the first and second sidewalls of silicon fin 164 a gate insulating material 172, such as a gate-oxide, is formed. Examples of suitable ways to form gate insulating material 172 include, but are not limited to, oxidation, deposition of high-k dielectric, or any combinations thereof. Examples of materials suitable for use in or for gate insulating material 172 include, but are not limited to, an oxide, high-k material, or any combinations thereof. The layer thickness for gate insulating material 172 is from about 0.7 nm to about 3 nm. Preferably, the layer thickness for gate insulating material 172 is from about 0.8 nm to about 2 nm. More preferably, the layer thickness for gate insulating material 172 is from about 0.8 nm to about 0.9

nm.

[0060] Referring to Figure 27, a gate layer 174 is deposited. Examples of suitable ways to deposit gate layer 174 include, but are not limited to, chemical vapor deposition. Examples of materials suitable for use in or for gate layer 174 include, but are not limited to, poly-silicon, poly-silicon/germanium, or any combinations thereof. The layer thickness for gate layer 174 is from about 50 nm to about 200 nm. Preferably, the layer thickness for gate layer 174 is from about 70 nm to about 150 nm. More preferably, the layer thickness for gate layer 174 is from about 100 nm to about 120 nm.

[0061] Referring to Figures 28 and 29, gate layer 174 has deposited thereon a second photoresist material 176. The second photoresist material 176 is patterned to define a gate region 186 thereunder for etching the gate material 174 and first insulating material 170 that is not part of the gate region 186 under the second photoresist material. The gate material 174 not covered by patterned second photoresist material 176 is removed. Examples of suitable ways to remove gate material 174 include, but are not limited to, RIE, dry etch, or any combinations thereof.

[0062] The first insulating material 170 not covered by patterned

second photoresist material 176 is removed. Examples of suitable ways to remove first insulating material 170 include, but are not limited to, RIE, dry etch, or any combinations thereof. Preferably, the removal of first insulating material 170 is done selective to the material of semiconductor substrate 102.

[0063] The second portion 126 of SiGe layer 104, as shown in Figure 27, is removed to produce a first void 178 having an upper boundary 180 defined by the lower surface of the second portion 124 of silicon layer 106 and a lower boundary 182 defined by a portion of the upper surface of the semiconductor substrate 102 that is underneath the second portion 124 of the silicon layer 106. The removal of the second portion 126 of SiGe layer 104 is preferably selective to the material of the semiconductor substrate 102 and the fin 124. Examples of suitable ways for removing second portion 126 of SiGe layer 104 include, but are not limited to, wet etching, dry etch, or any combinations thereof.

[0064] The structure provided by the gate layer 174, the gate insulating material 172, and first insulating material 170 suspend the second portion 124 of silicon layer 106 above the semiconductor substrate 120 with first void 178



in between.

[0065] Figure 29 shows a top view of a semiconductor structure at this stage of the method. The top surface 182 of semiconductor substrate 102 is sectioned by the fin structure 184 and gate region 186. The top surface of the fin structure 184 has material of the first blocking layer. The top surface of the gate region 186 has material of the second photoresist. Referring to Figures 28 and 29, beneath the intersection of the fin structure 184 and gate region 186, and between the suspended second portion 124 of silicon layer 106 and semiconductor substrate 102, is the first void 178.

[0066] Conventional processes for preparing a FinFET can be followed either leaving first void 178 as a void or filling first void 178 with an insulating material, such as an oxide, a nitride, or low-k material. Leaving first void 178 as a void provides a low capacitance. If the void is filled by nitride, the completed FinFET has high heat conduction to the substrate due to high thermal conductivity of nitride.

[0067] In another aspect of a method of the present invention, as shown in Figure 28, second photoresist material 176 can be removed before or after the creation of first void 178. Examples of suitable ways to remove second photoresist

material 176 include, but are not limited to, etching.

[0068] In another aspect of a method of the present invention, when leaving first void 178, as shown in Figure 28, as a void, it is preferred that the upper boundary 180, and optionally lower boundary 182, of first void 178 be re-oxidized to protect the lower surface of the second portion 124 of silicon layer 106. Figure 30 shows a cross sectional view and Figure 31 shows a top view of a semiconductor substrate at this stage of a method of the present invention. Figure 30 shows re-oxidized regions 190 and 192.

[0069] In yet another aspect of a method of the present invention, top surface 182 of semiconductor substrate 102, as shown in Figures 28 and 29, has deposited thereon a third insulating material. An examples of a suitable way to deposit third insulating material 188 includes HDP deposition in order to cover the surface of the substrate. Examples of suitable materials for use in or for third insulating material 188 include, but are not limited to, an oxide, nitride, or any combinations thereof. A preferred material for use in or for third insulating material 188 is an oxide. The layer thickness for third insulating material 188 can be from about 20 nm to about 50 nm.

[0070] The top surface of the fin structure 184 may also have deposited thereon third insulating material 188. A top surface of gate region 186 may also have deposited thereon third insulating material 188. Referring to Figures 30 and 31, beneath the intersection of the fin structure 184 and gate region 186, and between the suspended second portion 124 of silicon layer 106 and semiconductor substrate 102, is the first void 178.

[0071] The present invention has been described with particular reference to the preferred embodiments. It should be understood that the foregoing descriptions and examples are only illustrative of the invention. Various alternatives and modifications thereof can be devised by those skilled in the art without departing from the spirit and scope of the present invention. Accordingly, the present invention is intended to embrace all such alternatives, modifications, and variations that fall within the scope of the appended claims.